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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,515	02/24/2004	Chee-Wee Liu	D&F-040	8326

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,515	LIU ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (U.S. Patent No. 6,800,910). With regard to Claim 1, Lin discloses a Silicon FinFET (Fin Field Effect Transistor), (column 1, lines 13-15), comprising:

a substrate (column 4, line 27);

a strained silicon (column 4, line 43) in shape of a fin island located in said substrate (column 4, lines 43-44 and figure 4b);

a semiconductor (SiGe) embedded in said strained silicon (column 4, lines 43-44);

a dielectric layer (silicon oxide) formed on a surface of an intermediate section of said strained silicon (column 4, lines 55-58 and figure 4c); and

electrodes (column 4, lines 64-65) formed on said island and said dielectric layer (figure 4c).

With regard to Claim 2, Lin discloses a substrate that is an SOI (Silicon on Insulator) substrate (column 4, line 27).

With regard to Claim 3, Lin discloses a semiconductor (SiGe) that is employed for generating a strained silicon channel (column 2, lines 24-29).

With regard to Claim 4, Lin discloses a semiconductor consisting of a material (SiGe) suitable for producing strained silicon (column 2, lines 24-29 and column 4, lines 43-44).

With regard to Claim 5, Lin discloses surfaces of the intermediate section of the strained silicon covered by a dielectric layer (column 4, lines 55-58) comprising a left side, a right side, and top side surfaces of said intermediate section (figure 4c).

With regard to Claims 6-7, Lin discloses a dielectric layer that comprises an oxide layer (column 4, lines 55-57).

With regard to Claim 8, Lin discloses electrodes that are gate electrodes formed on a surface of said dielectric layer (column 4, lines 64-65), a source electrode formed on one terminal of said strained silicon; and a drain electrode formed on the other terminal of said strained silicon (column 5, lines 4-9).

With regard to Claim 9, Lin discloses a gate electrode selected from a group consisting of an n+ doped polysilicon gate electrode, a p+ doped polysilicon gate electrode, an n+ doped poly SiGe gate electrode and a p+ doped poly SiGe gate electrode (column 4, lines 64-67 and column 5, lines 4-9).

With regard to Claim 10, Lin discloses a strained silicon that conducting carriers (column 2, lines 24-29).

With regard to Claim 11, Lin discloses a conducting carrier that is one of an electron and a hole (column 2, lines 24-29 and column 4, lines 3-6).

With regard to Claim 12, Lin discloses a method for manufacturing a strained Silicon FinFET (column 4, lines 24-26), comprising:

(a) providing a substrate (column 4, line 27);

(b) forming a semiconductor (SiGe) layer on said substrate (column 4, line 28)

(c) forming a fin-shaped island (column 4, lines 41-42);

(d) forming a second silicon layer (column 4, lines 43-44) on a surface of said fin-shaped island;

(e) forming a dielectric layer on surfaces of said second silicon layer (column 4, lines 55-58) at an intermediate section of said fin-shaped island (figure 4c); and

(f) forming electrodes on said dielectric layer and fin-shaped island (column 64-65 and figure 4c).

With regard to Claim 13, Lin discloses a substrate that is an SOI (Silicon on Insulator) substrate (column 4, line 27).

With regard to Claim 14, Lin discloses a semiconductor (SiGe) that is employed for generating a strained silicon channel (column 2, lines 24-29).

With regard to Claim 15, Lin discloses a semiconductor consisting of a material (SiGe) suitable for producing strained silicon (column 2, lines 24-29 and column 4, lines 43-44).

With regard to Claim 16, Lin discloses a fin-shaped island that comprises a semiconductor layer and a first silicon layer (column 4, lines 43-44).

With regard to Claim 17, Lin discloses a method for forming a fin-shaped island that consists of etching (column 4, lines 33-42).

With regard to Claim 18, Lin discloses a surface of a fin-shaped island covered by a second silicon layer, that is the whole surface of the fin-shaped (column 4, lines 43-44 and figure 4c).

With regard to Claims 19-20, Lin discloses a dielectric layer that comprises an oxide layer (column 4, lines 55-57).

With regard to Claim 21, Lin discloses surfaces of the intermediate section of the strained silicon covered by a dielectric layer (column 4, lines 55-58) comprising a left side, a right side, and top side surfaces of said intermediate section (figure 4c).

With regard to Claim 22, Lin discloses electrodes that are gate electrodes formed on a surface of said dielectric layer (column 4, lines 64-65), a source electrode formed on one terminal of said strained silicon; and a drain electrode formed on the other terminal of said strained silicon (column 5, lines 4-9).

With regard to Claim 23, Lin discloses a gate electrode selected from a group consisting of an n+ doped polysilicon gate electrode, a p+ doped polysilicon gate electrode, an n+ doped poly SiGe gate electrode and a p+ doped poly SiGe gate electrode (column 4, lines 64-67 and column 5, lines 4-9).

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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